AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A semiconductor integrated circuit device comprising:

a MOS capacitor, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential, said power source wire is connected to a power source terminal, to which a first power source voltage is supplied, through a power source conversion circuit for converting said first power source voltage;

a ground terminal, to which said ground potential wire is connected; and

an electrostatic protection element connected in parallel with said MOS capacitor between said ground terminal and said MOS capacitor, said electrostatic protection element protecting said semiconductor integrated circuit device from electrostatic breakdown due to discharge of electric charge accumulated on said semiconductor integrated circuit device according to a charged device model,[[;]]

wherein, a wire resistance R1 of said ground potential wire between a connection point on said ground wire with one end of said electrostatic protection element and said ground terminal is larger than a wire resistance R2 of said ground potential wire between said connection point on said ground potential wire with one end of said electrostatic protection element and a connection point on said ground potential wire with the other end of said MOS

capacitor, wherein~~and said power source wire is connected to a power source terminal, to which a first power source voltage is supplied, through a power source conversion circuit for converting said first power source voltage~~

$V_C + R2 \bullet i < V_{OX}$

where V_C is a clamp voltage of said electrostatic protection element;

where V_{OX} is a dielectric breakdown voltage of said MOS capacitor;

where i a current flowing in R2; and

where R1 > zero and R2 > zero.

2. (*Withdrawn*) A semiconductor integrated circuit device comprising:

an electrostatic protection element, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential;

a ground terminal, to which said ground potential wire is connected; and

a MOS capacitor connected in parallel with said electrostatic protection element between said ground terminal and said electrostatic protection element;

wherein, a wire resistance of said ground potential wire between a connection point on said ground wire with one end of said MOS capacitor and said ground terminal is larger than a wire resistance of the ground potential wire between said connection point on said ground potential wire with one end of said MOS capacitor and a connection point on said ground potential wire with the other end of said electrostatic protection element.

3. (*Previously Presented*) A semiconductor integrated circuit device according to claim 1, wherein no other diffusion layer except said electrostatic protection element is connected on said ground potential wire between said ground terminal and the connection point on said ground potential wire with one end of the MOS capacitor.

4. (*Withdrawn*) A semiconductor integrated circuit device comprising:

an input/output terminal;

a first electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential;

a MOS capacitor, one end of which is connected to a power source wire for supplying the power source voltage and another end of which is connected to the ground potential wire; and

a second electrostatic protection element connected in parallel with said MOS capacitor between said first electrostatic protection element and said MOS capacitor;

wherein a wire resistance of the ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on the ground potential wire with one end of said second electrostatic protection element is larger than a wire resistance of the ground potential wire between the connection point on the ground potential wire with one end of said second electrostatic protection element and the connection point on the ground potential wire with the other end of said MOS capacitor.

5. (*Withdrawn*) A semiconductor integrated circuit device comprising:

an input/output terminal;

a first electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential;

a second electrostatic protection element, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying the ground potential; and

a MOS capacitor connected in parallel with said second electrostatic protection element between said first electrostatic protection element and said second electrostatic protection element;

wherein a wire resistance of the ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on the ground potential wire with one end of said MOS capacitor is larger than a wire resistance of the ground potential wire between the connection point on the ground potential wire with the one end of said MOS capacitor and the connection point on the ground potential wire with the other end of said second electrostatic protection element.

6. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein no other diffusion layer except said first electrostatic protection element is connected on said ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on said ground potential wire with one end of the MOS capacitor.

7. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, comprising:

a first and second commonly connected ground potential wires for supplying a ground potential and an input/output terminal;

an electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to said first ground potential wire; and

a MOS capacitor, one end of which is connected to the power source wire for supplying the power source voltage and another end of which is connected to said second ground potential wire;

wherein, said second ground potential wire is not connected to the input/output terminal and a diffusion layer is connected to said second ground potential wire between said ground terminal and the connection point on said second ground potential wire with the other end of said MOS capacitor.

8. (*Previously Presented*) A semiconductor integrated circuit device according to claim 1, wherein said power source wire is connected to a power source terminal, to which a predetermined power source voltage is supplied.

9. (*Cancelled*).

10. (*Currently Amended*) A semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element clamps a voltage applied across said ground terminal and said power source wire at the ~~a~~ clamp voltage, which is lower than the dielectric breakdown voltage of said MOS capacitor.

11. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein said second electrostatic protection element clamps a voltage applied to both terminals at a clamp voltage, which is lower than the dielectric breakdown voltage of said MOS capacitor.

12. (*Previously Presented*) A semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a MOS field effect transistor, a drain of which is connected to said power source wire, and a source and a gate of which are connected to said ground potential wire.

13. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein said second electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the gate of which are connected to said ground potential wire.

14. (*Cancelled*).

15. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein said second electrostatic protection element is a bipolar transistor, constituted by forming on a substrate having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.

16. (*Cancelled*).

17. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein said second electrostatic protection element is a thyristor, constituted by forming on a substrate having a first conductive type two diffusion layers respectively having a first conductive type and a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other, and by further forming on a well having the second conductive type formed on said substrate having the first conductive type two diffusion layers respectively having the first conductive type and the second conductive type, so as to closely face each other.

18. (*Cancelled*).

19. (*Withdrawn*) A semiconductor integrated circuit device according to any one of claims 4 or 5, wherein said second electrostatic protection element is a diode, constituted by forming on a substrate or a well having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.

20. (*Not Entered*) A semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a diode, constituted by forming on a substrate or a well having a first conductive type two diffusion layers having a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each other.

21. (*Currently Amended*) A semiconductor integrated circuit device comprising:

a power source wire;

a ground terminal;

a MOS capacitor comprising first and second terminals, wherein said first terminal is connected to a power source wire, wherein said power source wire is connected to a power source terminal and a first power source voltage is supplied through a power source conversion circuit for converting said first power source voltage;

a ground potential wire connected between said ground terminal and said second terminal

of said MOS capacitor, wherein said ground potential wire further comprises a connection point disposed between said ground terminal and said second terminal of said MOS capacitor such that the wire resistance between said ground terminal and said connection point is greater than the wire resistance between said second terminal and said connection point; and

an electrostatic protection element connected between said power source wire and said connection point so that said electrostatic protection element is in parallel with said MOS capacitor, said electrostatic protection element protecting said semiconductor integrated circuit device from electrostatic breakdown due to discharge of electrostatic charge accumulated on said semiconductor integrated circuit device according to a charged device model, wherein

$V_C + R2 \cdot i < V_{OX}$

where V_C is a clamp voltage of said electrostatic protection element;

where V_{OX} is a dielectric breakdown voltage of said MOS capacitor;

where i a current flowing in R2; and

where R1 > zero and R2 > zero.

22. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein no other diffusion layer except said electrostatic protection element is connected on said ground potential wire between said ground terminal and said connection point on said ground potential wire.

23. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein said power source wire is connected to a power source terminal to which a predetermined power source voltage is supplied.

24. (*Cancelled*).

25. (*Currently Amended*) The semiconductor integrated circuit device according to claim 21, wherein said electrostatic protection element clamps a voltage applied across said ground terminal and said power source wire at the ~~a~~ clamp voltage, said clamp voltage being lower than a dielectric breakdown voltage of said MOS capacitor.

26. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein said electrostatic protection element is a MOS field effect transistor, a drain of which is connected to said power source wire, and a source and a gate of which are connected to said ground potential wire.

27. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein said electrostatic protection element is a bipolar transistor.

28. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein said electrostatic protection element is a thyristor.

29. (*Previously Presented*) The semiconductor integrated circuit device according to claim 21, wherein said electrostatic protection element is a diode.

30. (*Previously Presented*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a bipolar transistor.

31. (*Previously Presented*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a thyristor.

32. (*Previously Presented*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a diode.

33-34. (*Cancelled*).